REMARKS

Claims 1-22 are pending in the present application. Claim 16 was amended to correct a typographical error. No new matter has been added to the amended claim. Reconsideration of the claims is respectfully requested.

Claim Rejections - 35 USC § 112

Claims 19 and 22

Claims 19 and 22 were rejected under 35 U.S.C 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. (Office Action at page 2).

Claim 19 recites, among other limitations, a "silicon substrate having (100) crystal orientation." Claim 22 also recites, among other limitations, the same limitation. The Applicants respectfully submit that this limitation is implicit in the specification.

M.P.E.P. § 2163 states that "[w]hile there is no *in haec verba* requirement, newly added claim limitations must be supported in the specification through express, implicit, or inherent disclosure. (M.P.E.P at page 2100-157, column 2, emphasis added.) Although the exact words, "(100) crystal orientation" do not appear in the specification, the use of a silicon substrate with this orientation is implicit in the specification. The specification, at page 1 for example, discloses that "integrated circuits are fabricated on a slice or wafer, of single-crystal (monocrystalline) silicon, commonly termed a 'bulk' silicon wafer." As shown in Table 1-3: Specifications for Single-Crystal Silicon Wafers, page 27 of S. Wolf, Silicon Processing for the VLSI Era (Volume 1), Lattice Press (2000), inserted below this paragraph, for wafers from 150 to 300 mm in diameter, the industry standard surface orientation is the (100) crystal orientation. As stated in the M.P.E.P. § 2163, "an inventor is not required to describe every detail of his invention.

An applicant's disclosure obligation varies according to the art to which the invention pertains. (M.P.E.P. at page 2100-163, column 2). "Generally, there is an inverse correlation between the level of skill and knowledge in the art and the specificity of disclosure necessary to satisfy the written description requirement. Information which is well known in the art need not be described in detail in the specification. See, e.g., *Hybritech, Inc. v. Monoclonal Antibodies, Inc.*, 802 F.2d 1367, 1379-80 (Fed. Cir. 1986)." (M.P.E.P. at page 2100-160, column 2). In this case, as demonstrated by Table 1-3 from Wolf, the use of single-crystal silicon wafers with (100) crystal orientation is a well known semiconductor industry standard. Therefore, because one skilled in the art of fabricating integrated circuits on silicon wafers would know that "a silicon substrate having (100) crystal orientation" is an industry standard, the Applicants submit that the disclosure of the claimed orientation is implicit in the specification.

Table 1-3 SPECIFICATIONS FOR SINGLE-CRYSTAL SILICON WAFERS

Parameter	150 mm	200 mm	300 mm
Diameter (mm)	150 ± 0.2	200 ± 0.2	300 ± 0.1
Thickness (μm)	675 ± 25	725 ± 20	775 ± 25
Primary flat length (mm)	55–60	notch	notch
Oxygen content (ASTM '79) (ppma)		≥ 23 ± 2	≥ 22 ± 1.5
Flatness (μm) (GTIR)	1.5	1.5	1.5
Site Flatness (μm) (SFQD)		± 0.17 (1998)	± 0.12 (2001)
Surface orientation	(100)	(100)	(100)

<u>Claims 20 and 22</u>

Claims 20 and 22 were rejected under 35 U.S.C. § 112 for reciting, "silicon-containing-deposition species." The examiner states that to the extent "Applicants' intend to claim species other than SiH_4, $Si_xCl_yH_z$ and $SiCl_x$, those [other] species were not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention." (Office Action at page 2-3). Claim 21, which

depends on claim 20 was also rejected for at least this reason. The Applicants respectfully traverse this rejection.

The specification discloses that "deposition may occur by way of a silicon bearing compound such as silanes, e.g., $Si_xCl_yH_z$,, SiH_4, $SiCl_x$, and other silicon compounds." (Specification at page 22). The Federal Circuit has held that "limitations from the specification are not to be read into the claims." Because "claims are interpreted in light of the specification does not mean that everything expressed in the specification must be read into all the claims. *Teleflex, Inc. v. Ficosa N. Am. Corp.*, 299 F.3d 1313, 1326 (Fed. Cir. 2002) (internal citations omitted). Therefore, the claims should not be limited to the embodiments listed in the specification, which are given as examples of silicon bearing compounds. On the contrary, the "other silicon compounds" language found in the specification provides support, at the least, for the broader claim language of "silicon-containing-deposition species" as recited, in part, in claims 20 and 22.

Claim 21

Claim 21 was rejected for reciting, "wherein the combination of the deposition species and the etching species are contacting the non-uniform surface in a thermal setting of a temperature of about 1,000 degrees Celsius or greater." (Office Action at page 3). The examiner states that claim 2, which recites, in part, "said thermal setting increases a temperature of said non-uniform surface to about 1,000 degrees Celsius and greater" has a "completely different scope than the presently recited claim 21." (Office Action at page 3). The Applicants respectfully submit that the limitations of both claims 2 and 21 are disclosed in the specification.

The specification states "The thermal treatment can be from a furnace, but is preferably from a rapid thermal processing tool such as an RTP tool. Alternatively, the tool can be from an epitaxial chamber, which has lamps for rapidly heating a substrate." (Specification at page 23, emphasis added).

The first sentence of this quote provides support, for example, for claim 21, which recites, in part, "wherein the combination of the deposition species and the

etching species are contacting the non-uniform surface in a thermal setting of a temperature of about 1,000 degrees Celsius or greater." A furnace or an RTP tool will heat the environment in which the substrate is placed as well as the substrate. In operation, the wafers are placed in the furnace and the temperature in the furnace is slowly ramped (over a period ranging from several minutes to tens of minutes) to the process temperature. See S. Wolf, Silicon Processing for the VLSI Era (Volume 1, 2nd Edition), Lattice Press (2000), pages 304-313. The second sentence of the quote from page 23 of the specification discloses the alternative of heating a substrate in an epitaxial chamber. This sentence, therefore, provides support for the claim limitations found in claim 2. Therefore, the Applicants respectfully submit that support is found in the specification for both claims 2 and 21.

Claim Rejections - 35 USC § 103

Claims 1-13

Claims 1-13 were rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5, 869,387 to Sato et al. (hereafter Sato). The examiner states that all the recited limitations of claim 1 are taught by Sato since Sato teaches a deposition species for deposition of a deposition material (Office Action at page 5), the etching species contacting the non-uniform surface (Office Action at page 6), and the thermal setting to reduce a level of non-uniformity of the non-uniform surface by filling a portion of the defects to smooth the film material (Office Action at page 7). The Applicants respectfully submit that even if these steps are present in Sato, Sato provides no motivation to apply a "combination" of these steps "to reduce a level of non-uniformity of the non-uniform surface by filling a portion of the defects to smooth the film of material" as recited, in part, in claim 1.

Deposition

Sato discloses that "a thin monocrystal layer 202 is formed on the porous [Si] substrate surface by epitaxial growth." (Sato at column 9, lines 45-46). However,

the "thin monocrystalline layer which is grown epitaxially on the porous Si, may have a rough surface." (Sato at column 9, line 66). Thus, Sato teaches that "after the thin monocrystal layer is formed on the porous layer, the substrate having the thin monocrystal layer formed thereon is heat-treated in a reducing atmosphere to flatten the surface of the thin monocrystalline Si layer." (Sato at column 10, lines 6-12). Therefore, Sato does not employ the deposition process to smooth a non-uniform layer.

Etching

Sato discloses that after bonding the epitaxially grown Si layer on the porous Si layer to a another substrate, the porous Si layer is entirely removed by chemical etching. (Sato at column 10, lines 17-20, and lines 37-38). Once again, Sato teaches etching of the porous Si layer, not "to reduce a level of non-uniformity of the non-uniform surface by filling a portion of the defects to smooth the film of material" as recited, in part, in claim 1, but to expose the monocrystalline layer for subsequent processing into dielectrically isolated electronic elements. (Sato at column 11, lines 38-39).

Therefore, because Sato does not teach or suggest that either the deposition or etching steps reduce the level of non-uniformity of a non-uniform surface, there is no motivation to combine these separate processing steps to achieve the method of the present invention. That is, a person skilled in the art would not be motivated to combine two non-smoothing process steps to arrive at a smoothing process step based on the information disclosed in Sato.

Applicants submit that claim 1 is in a condition for allowance. Claims 2-13, which depend from claim 1, should be allowed for at least a similar rationale as discussed for allowing claim 1, and others.

Claim 19

Claim 19 was rejected because Sato, on page 2, provides a reference to Cai, Tianhai, "Elimination of stacking faults in a silicon epitaxial layer of (100)

orientation by heat treatment", *Journal of Applied Physics*, 1 Jun. 1990, USA, vol. 67, nr. 11, pp. 7176-7178.

Claim 19, which depends from claim 1, should be allowable for at least a similar rationale as discussed for allowing claim 1, and others.

Claims 20-22

Claims 20-22 were rejected based on similar arguments to those given above. In particular, the examiner, citing In re Tatincloux, 108 USPQ 125 (CCPA 1955) stated that the "performance of two steps simultaneously, which have previously been performed in sequence was held to have been obvious." However, the exception provided for in Tatincloux and acknowledged by the examiner applies when the combination of two previously sequential steps produces new or unexpected results. (Office Action at page 8). The Applicants respectfully submit that the combination of steps recited in claims 20 and 22 meet the requirements of this exception.

As stated above, Sato does not teach or suggest that the deposition or etching processes are performed "to smooth the surface" as recited, in part, in claim 20 or "to smooth and reduce a level of non-uniformity of the non-uniform surface" as recited, in part, in claim 22. On the contrary, Sato discloses a deposition process that requires subsequent thermal treatment to flatten the surface and an etch process that merely removes unwanted porous Si material. Because the combination of these steps produces a new result, for example, smoothing during deposition, the Applicants submit that this combination is not obvious.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance and an action to that end is urged. If the Examiner believes a telephone conference would aid in the prosecution of this case in any way, please call the undersigned at 650-326-2400.

PATENT

Respectfully submitted,

Steve Y. Cho
Reg. No. 44.612

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
Tel: 650-326-2400
Fax: 415-576-0300
RTO:ccl
PA 3277357 v1

PATENT

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Claim 16 has been amended as follows:

16. (Amended) The method of claim 1 wherein said deposition species comprise a species selected from SiH_4, **[SixClyHz]** $\underline{Si_xCl_yH_z}$, and **[SiClx]** $\underline{SiCl_x}$.

All pending claims are reproduced below for the Examiner's convenience.

1. A method of fabricating substrates, the method comprising

providing a substrate comprising a film of material characterized by a non-uniform surface, the non-uniform surface including a plurality of defects, at least some of the defects being of a size ranging from about 100 Angstroms and greater; and

applying a combination of a deposition species for deposition of a deposition material and an etching species for etching an etchable material, the combination of the deposition species and the etching species contacting the non-uniform surface in a thermal setting to reduce a level of non-uniformity of the non-uniform surface by filling a portion of the defects to smooth the film of material, the film of material being substantially free from the defects and being characterized by a surface roughness of a predetermined value.

2. The method of claim 1 wherein said thermal setting increases a temperature of said non-uniform surface to about 1,000 Degrees Celsius and greater.

3. The method of claim 2 wherein said temperature increases is about 10 Degrees Celsius per second and greater.

4. The method of claim 2 wherein said temperature increases is about 20 Degrees Celsius per second and greater.

5. The method of claim 1 wherein said non-uniform surface comprises a plurality of particles therein, the particles comprising a hydrogen bearing species.

6. The method of claim 5 wherein said plurality of particles are derived from hydrogen gas during an implantation process.

7. The method of claim 1 wherein said predetermined value is less than about two nanometers root mean square.

8. The method of claim 1 wherein said predetermined value is less than about 1 nanometers root mean square.

9. The method of claim 1 wherein said predetermined value is less than about 0.1 nanometer root mean square.

10. The method of claim 1 wherein said etching species comprise a hydrogen bearing compound.

11. The method of claim 1 wherein said etching species comprise a halogen bearing compound.

12. The method of claim 1 wherein said etching species comprise a fluorine bearing compound.

13. The method of claim 12 wherein said fluorine bearing compound is selected from SF_6, CF_4, NF_3, and CCl_2F_2.

14. The method of claim 1 wherein said deposition species comprise a silane bearing gas.

15. The method of claim 1 wherein said deposition species comprise a silicon bearing species.

16. (Amended) The method of claim 1 wherein said deposition species comprise a species selected from SiH_4, $Si_xCl_yH_z$, and $SiCl_x$.

17. The method of claim 1 wherein the non-uniform surface is a cleaved surface, the cleaved surface being made from a process selected from a controlled cleaving action, a Smart Cut™ process, or an ELTRAN™ process.

18. The method of claim 1 wherein the defects are called HF defects.

19. The method of claim 1, wherein the substrate is a silicon substrate having (100) crystal orientation.

20. A method of fabricating substrates, the method comprising

providing a substrate comprising a film of material with a non-uniform surface, the non-uniform surface including a plurality of defects, at least some of the defects being 100 Angstroms or greater; and

applying simultaneously to the non-uniform surface a combination of a silicon-containing-deposition species for deposition of a deposition material and a halogen-containing-etching species for etching an etchable material in order to smooth the surface.

21. The method of claim 20, wherein the combination of the deposition species and the etching species are contacting the non-uniform surface in a thermal setting of a temperature of about 1,000 degrees Celsius or greater.

22. A method of fabricating substrates, the method comprising

providing a silicon substrate comprising a film of material with a non-uniform surface, the non-uniform surface including a plurality of defects, at least some of the defects being 100 Angstroms or greater, the silicon substrate having (100) crystal orientation, the non-uniform surface including particles derived from hydrogen gas during an implantation process; and

applying simultaneously to the non-uniform surface a combination of a silicon-containing-deposition species for deposition of a deposition material and a halogen-containing-etching species for etching an etchable material in order to smooth and reduce a level of non-uniformity of the non-uniform surface, the halogen-containing-etching species including HCl.